Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Please cancel claim 1 without prejudice and substitute the following new claims:

37. (new) An integrated semiconductor structure comprising:

a multijunction solar cell structure having at least first and second subcells; and a bypass device having p-type, i-type, and n-type layers integral to subcell to prevent reverse biasing when a solar cell is shadowed.

38. (new) The structure as defined in claim 37, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass device is a bypass diode formed on a second portion of the substrate.

39. (new) The structure as defined in claim 38, wherein the subcells are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown in a subsequent second process.

40. (new) The structure as defined in claim 39, wherein such expitaxially grown diode is electrically connected across at least said first and second subcells to protect such first and second subcells against reverse biasing.

41. (new) The structure as defined in claim 39, wherein the bypass diode includes a metal/semiconductor contact.

42. (new) The structure as defined in claim 41, wherein the metal/semiconductor contact is TiAu with InGaP.

43. (new) The structure as defined in claim 41, wherein the metal/semiconductor contact forms a Schottky junction.

44. (new) The structure as defined in claim 38, wherein the substrate is Ge.

45. (new) The structure as defined in claim 37, wherein the second solar subcell is fabricated as least in part with InGaP.

46. (new) The structure as defined in claim 37, wherein the first solar subcell is fabricated at least in part with GaAs.

47. (new) A solar cell semiconductor devise comprising:

a semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell; and

a second region laterally spaced apart from said first region and in which

the sequence of layers forms a support for an integral bypass diode to protect said cells against reverse biasing.

48. (new) A device as defined in claim 47, wherein the sequence of layers of said one cell and the sequence of layers of the bypass diode are epitaxially grown in the same process step.

49. (new) A device as defined in claim 47, wherein the semiconductor body includes a Ge substrate, and at least one of the solar cells is fabricated at least in part with GaAs.

50. (new) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell; and a second region including a sequence of layers that forms a bypass diode to protect said cell against reverse biasing; and

a lateral conduction layer lying over said layers of said first region for electrically connecting the multijunction solar cell to said bypass diode.

51. (new) A device as defined in claim 50, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass

diode is formed on a second portion of the substrate over said lateral conduction layer.

52. (new) A device as defined in claim 50, wherein the solar cell and lateral conduction layer are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown in a subsequent second process.

53. (new) A device as defined in claim 50, wherein such epitaxially grown diode is electrically connected across at least said first and second subcells to protect such first and second subcells against reverse biasing.

54. (new) A device as defined in claim 50, wherein the bypass diode includes a metal/ semiconductor contact.

55. (new) A device as defined in claim 54, wherein the metal/semiconductor contact is TiAu with InGaP.

56. (new) A device as defined in claim *54,* wherein the metal/semiconductor contact forms a Schottky junction.

57. (new) A device as defined in claim 50, wherein said bypass diode includes p-type, and n-type layers.

58. (new) A solar cell semiconductor device comprising:

a semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiçonductor material forms a sequence of cells of a multijunction solar cell; and a second region separated by a well in said sequence of layers from said first region and in which the sequence of layers forms a support for an integral bypass diode to protect the multijunction solar cell against reverse biasing.

59. (new) A device as defined in claim 58, wherein the sequence of layers said one cell and the sequence of layers of the bypass diode are epitaxially grown in the same process step.

60. (new) A device a defined in claim 58, wherein the semiconductor body includes a Ge substrate, and at least one of the cells is fabricated at least in part with GaAs.

61. (new) A device as defined in claim 58, further comprising

a lateral conduction layer lying over said layers of said first region for electrically connecting the multijunction solar cell to said bypass diode.

62. (new) The device as defined in claim 61, wherein said structure includes a substrate, wherein the subcells are fanned on a first portion of the substrate and said bypass diode is formed on a second portion of the substrate over said lateral conduction layer.

63. (new) The device as defined in claim 61, wherein the solar cell and lateral conduction layer are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown in a subsequent second process.

64. (new) The device as defined in claim 59, wherein such epitaxially grown diode is electrically connected across at least said first and second subcells to protect such first and second subcells against reverse biasing.

65. (new) The device as defined in claim 58, wherein the bypass diode includes a metal/semiconductor contact.

66. (new) The device as defined in claim 65, wherein the metal/semiconductor contact is TiAu with InGaP.

67. (new) The device as defined in claim 65, wherein the metal/semiconductor contact forms a Schottky junction.

68. (new) The device as defined in claim 61, wherein said bypass diode includes p-type, i-type, and n-type layers.

69. (new) The device as defined in claim 61, wherein the lateral conduction layer is an n-doped GaAs for conducting electrical current.

70. (new) The solar device of claim 68, wherein the p-type layer of the bypass diode is a p-doped GaAs layer and the n-type layer of the bypass diode is an n-doped GaAs layer.

71. (new) The solar device of claim 68, wherein the i-type layer is a lightly doped GaAs layer for reducing defect breakdown.

72. (new) The solar device of claim 68, wherein the i-type layer is an undoped GaAs layer for reducing defect breakdown.

73. (new) A solar cell semiconductor device comprising:

a substrate;

a first sequence of layers of semiconductor material deposited on said substrate; including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell; and a second region including said first sequence of layers, and a second sequence of layers that forms a bypass diode to protect said cell against reverse biasing; and

a metal layer deposited on a portion of said substrate and over at least a portion of said second region for electrically shorting the first sequence of layers of said second region and to electrically connect to said bypass diode in said second region.

74.. (new) A device as defined in claim 73, wherein said metal layer forms a shunt having a first contact on the solar cell and a second contact on the bypass diode, wherein the first contact is connected to the substrate and the second contact of the shunt is connected to a lateral conduction layer.

75. (new) A device as defined in claim 73, further comprising a well situated between the solar cell and the bypass diode that provides electrical isolation between the solar cell and the diode.

76. (new) A device as defined in claim 74, further comprising a stop etch layer deposited over the lateral conduction layer.

77. (new) A device as defined in claim 73, wherein said bypass diode includes p-type, i-type, and n-type layers.

78. (new) A device as defined in claim 74, wherein the lateral conduction layer is an n-doped GaAs layer for conducting electrical current.

79. (new) A solar divide of claim 77, wherein the p-type layer of the bypass diode is a p-doped GaAs layer and the n-type layer of the bypass diode is an n-doped GaAs layer.

80. (new) A solar device of claim 77, wherein the i-type layer is a lightly doped GaAs layer for reducing defect breakdown.

81. (new) A solar device of claim 77, wherein the i-type layer is an undoped GaAs layer for reducing defect breakdown.

82. (new) A method of making an integrated semiconductor structure comprising:

forming a multijunction solar cell structure having at least first and second subcells; and

subsequently forming and a bypass device having p-type, i-type, and n-type layers integral to a subcell to prevent reverse biasing when a solar cell is shadowed.

83. (new) The method as defined in claim 82, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass device is a bypass diode formed on a second portion of the substrate.

84. (new) The method as defined in claim 83, wherein the subcells are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown in a subsequent second process.

85. (new) The method as defined in claim 84 further comprising electrically connecting the bypass diode across at least said first and second subcells to protect such first and second subcells against reverse biasing.

86. (new) The structure as defined in claim 83, further comprising forming a metal/semiconductor contact on the bypass diode to form a Schottky junction

87. (new) A method of making a solar cell semiconductor device comprising:

depositing a sequence of layers of semiconductor material on a substrate including forming a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell; and

forming a second region laterally spaced apart from said first region and which the sequence of layers forms a support for an integral bypass diode to protect said cells against reverse biasing.

88. (new) A method as defined in claim 87, wherein depositing the sequence of layers of said solar cell and the sequence of layers of the bypass diode are performed by epitaxial growth in the same process step.

89. (new) A method as defined in claim 87, further comprising providing a Ge substrate, and fabricating at least one of the solar cells in the Ge substrate.

90. (new) A method of making a solar cell semiconductor device comprising:

providing a substrate;

Depositing a sequence of layers of semiconductor material said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell; and a second region in which the sequence of layers forms a bypass diode to protect said cell against reverse biasing; and

Depositing a lateral conduction layer over said layers of said first region for electrically connecting the multijunction solar cell to said bypass diode.

91. (new) A method as defined in claim 90, further comprising forming the subcells on a first portion of the substrate and forming said bypass diode on a second portion of the substrate over said lateral conduction layer.

92. (new) A method as defined in claim 90, further comprising growing the solar call and the lateral consuction layer in a first process and growing the active layers of said bypass diode in a subsequent second process.

93. (new) A method as defined in claim 90, further comprising connecting the bypass diode across at least first and second subcells of said multifunction solar cell to protect such first and second subcells against reverse biasing.